Mask Designer Resume

★★★★★ 2.00 /5 (Submit Your Rating)

Austin, TX

TECHNICAL SKILLS

- 15 years experience in physical design, EDA/CAD, IC layout mask design and verification of high performance, deep Submicron CMOS/BiCMOS digital, analog, and Mixed Signal SoC.
- Expert in layout floor planning and power planning, place and route of large digital and analog blocks, standard cell planning, hierarchical layout assembly, device matching and sizing, pad ring/ flip-chip and through-via geometries creation, post layout extraction, static and dynamic analyses, power analyses, design closure, DFM and E-beam mask generation, reticle fabrication.
- Experienced in EDA/CAD Engineering, Physical Design Verification Methodology and adaptation/creation of PDK in Cadence/CALIBRE environment. Able to create CALIBRE DRC/LVS decks.
- Experienced in layout design of specific components/cells/IP including inductors, low noise, low power resistors, capacitors, pad IOs, ESD structures, data paths, bit cell array, opamp, PLL, DAC, ADC.
- Good knowledge of SUN/UNIX platform (Cadence Virtuoso XL 5.1 and 6.1, GENESYS, LTL- 100, Allegro, CALIBRE, HERCULES, DRACULA, DIVA, ASSURA, HSPICE, VERILOG, Cadence SoC Encounter RTL-to-GDSII), and PC/WINDOWS platform (EDA TANNER L- Edit Pro 10, AUTOCAD, WORKBANCH, MULTISIM, MATLAB, SANDIA Ultra - planer Multi - level MEMS design, OFFICE).
- Programming/scripting: UNIX, C++, PERL, TCL and SKILL.
- Previous experience in mask design for deep submicron silicon processing (90nm, 65nm, 45/40nm, 28nm). Familiar with technologies and design kits of different founders (TSMC, UMC, Chartered Semiconductor) and physical design methodologies and documentation of different companies (Lattice, IBM, Intel, Maxim, Qualcomm, Cirrus Logic), including the new photo/litho processing: double patterning, self-aligned spacer, 2D layout consideration, OPC, reticle/mask fabrication , through Si stacking for 3D chip packaging.
- Able to solve layout dependent proximity effects/failure issues in deep Submicron CMOS: well proximity, STI stress/strain, OPC, metal fill impacts, star connection impedance discontinuity, latch up, antenna, electro migration, RC delay, ESD, self heating and cross capacitance.

PROFESSIONAL EXPERIENCE

Sr. Mask Designer

Confidential, Hudson, MA. 02/2012 - 04/2012 (contract).

Consulting in mask design of CMOS test chip with RF components, using Cadence VXL5.1 and CALIBRE.

Support Engineer 4 07/2011 - 01/2012 (contract)

Confidential, San Diego, CA

Consulting in mask design of CMOS mixed signal IC using Cadence 6.1,VXL, CALIBRE, and internal tools for advanced mobile DRAM architecture based on 65 and 40 nm technologies.

Sr. Mask Designer 01/2011 - 06/2011 (contract)

Confidential, Hillsboro, OR

Consulting in mask design of CMOS mixed signal IC using Cadence 6.1, VXL, CALIBRE, and internal rules for 45 and 28nm technologies.

Sr. Layout Verification Engineer

Confidential, NY 09/2009 - 11/2009 (contract)

Consulting in layout design of nano-photonics components/cells using CMOS/Cadence/Hercules environment. Developed the physical design verification and extraction tools. Created nano-photonics standard cells library.

Sr. Mask Designer

Confidential, Chandler AZ. 01/2008 - 01/2009 (contract).

Full-custom CMOS digital IC mask design using Cadence VXL, GENESYS, HERCULES, CALIBRE, HSPICE.

Sr. Mask Designer

Confidential, Austin Design Center, TX. 07/2006 - 12/2007 (contract)

Full-custom IC mask design on cell, block and top levels, including tape out for 2P3M mixed signal BICMOS 125nm technology using LTL-100 layout editor and Hercules/Calibre tools for verification.

Sr. Analog/RF Mask Designer

Confidential, Chandler AZ. 10/2005 - 07/2006 (contract).

Full-custom analog/ RF/mixed signal mask design using VXL, HERCULES, ASSURA, CALIBRE, HSPICE. Designed layout for a series of OPAMP, LNA, mixers and filters on cell, block and chip levels on 90nm node.

Sr. MP Mask Designer

Confidential, Cary, NC. 10/2004 - 10/2005, (contract).

Full-custom 65nm/1P/6M digital IC Physical design including cell, block and top levels for 3G CDMA wireless communications products using VXL, CALIBRE, HERCULES and H-SPICE.

Physical Designer

Confidential, Austin, TX. 07/2002 - 10/2004,

Performed consulting services in IC, PCB and MEMS physical design using VIRTUOSO, CALIBRE, ALLEGRO, SPECTRA, HSPICE, ORCAD, AUTOCAD, and SANDIA Ultra - planer Multi - level MEMS design.

Device Engineer-2

Confidential, Austin, TX. 10/2001 - 07/2002

Developed physical design verification methodology for 0.35um 3.3V/5V 2P5M mixed signal CMOS process, 0.25um 2.5V/3.3V 1P5M logic CMOS process and 0.18um 1.8V/3.3V 1P6M mixed signal CMOS process. Created generic topological layout rules and CALIBRE DRC/LVS decks compatible with UMC, TSMC and Chartered SM. Designed test suits for DRC/LVS decks debugging including analog cells OPAMP, VGA, PLL, ADC, OTA.

CAD instructor

Confidential, 09/1992 - 08/1999. (Relocation in USA)

Lectured in Russian and Romanian languages the course on CAD VLSI.

Reticle/Mask production Manager Confidential, Chisinau, Moldova. 09/1982 - 08/1992.

EDUCATION / TRAINING

- **MS**. Electrical Engineering with a focus in Microelectronics and Microprocessor Systems
- **BS**. Electrical Engineering. Major Semiconductor Devices.
- **Certificate.** Mentor Graphics Corporation
- **Certificate.** Mentor Graphics Corporation
- **Certificate**. Austin Community College, TX. CMOS IC / PCB layout and design. 2003.
- **Training.** Intel Corporation, Folsom, CA. Flash memory mask design, 0.09u, VXL/VCR, STX CADWARE, Avanti/Hercules. 2004.
- **Training**. Austin Community College, TX. AUTOCAD & SANDIA Ultra-planer Multi-level MEMS design. 2004
- **Training**. Intel Corporation, Chandler, AZ. Analog/Mixed signal mask design, using GENESYS, 2008

PUBLICATIONS

- 15 publications in Russia related to IC physical design, component modeling, mask/reticle fabrication, and lithography processing.
- Flat color display device and method of manufacturing. Patent application publication US2004/0207309A1. Oct.21, 2004.

LEGAL STATUS

- USA citizen